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(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Mail Stop 525, Boise, ID 83707-0006 (US).

(72) Inventor: SEYYEDY, Mir, Majid; 4665 North Bantry Place, Boise, ID 83702 (US).

(74) Agent: VIKSNINS, Ann, S.; Schwegman, Lundberg & Woessner, P.O. Box 2938, 3500 IDS Center, 80 South Eighth Street, Minneapolis, MN 55402 (US).

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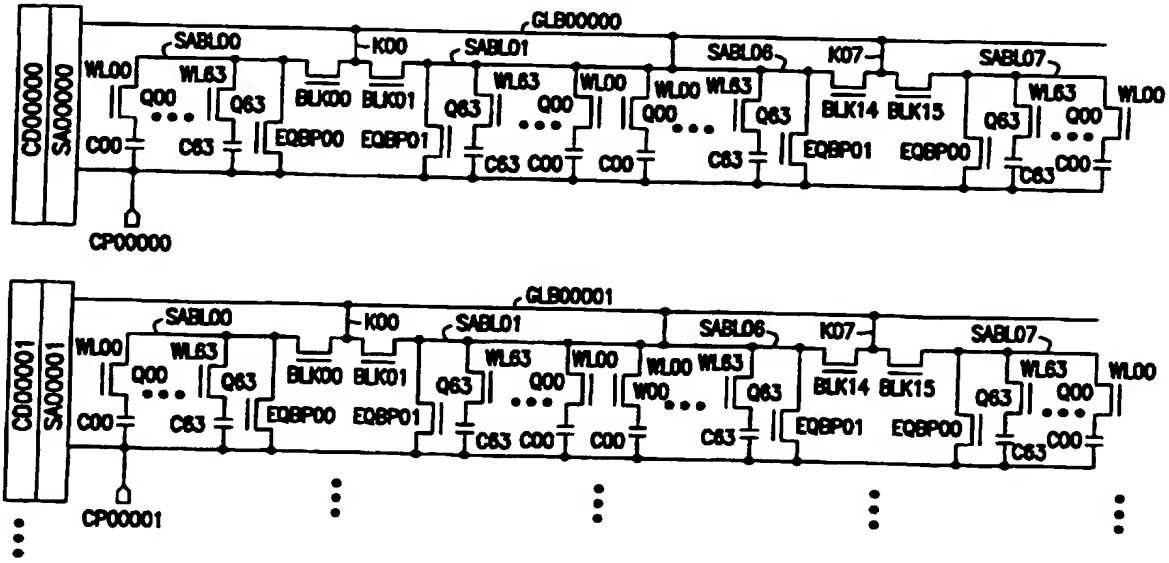

(57) Abstract

An integrated memory array circuit, such as a DRAM, has global array bit lines each of which is connected hierarchically above a plurality of electrically isolatable subarray bit lines. Each subarray bit line is connected hierarchically above a plurality of memory cells. The memory cells are selectively coupled to the subarray bit lines using word lines. Data stored on the memory cells can be left floating, or can be refreshed in temporary storage on both the global array bit lines and the electrically isolatable subarray bit lines which have sufficient capacitance to maintain readily accessible data in temporary storage.

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Memory Circuit with Hierarchical Bit Line Structure

Technical Field of the Invention

This invention generally relates to semiconductor integrated circuit memory structures and, more precisely, relates to a memory array having global array bit lines each of which is connected hierarchically above a plurality of electrically isolatable subarray bit lines, each subarray bit line being connected hierarchically above a plurality of memory cells, each memory cell being in communication with a corresponding word line, where data can be left floating and can be refreshed in temporary storage on both the global array bit lines and the electrically isolatable subarray bit lines which have sufficient capacitance to maintain readily accessible data in temporary storage.

Background of the Invention

In dynamic random access memory chips, bit line capacitance is an important consideration. A reduction in bit line capacitance reduces the amount of power required by the memory cell structure. Attempts have been made to optimize or maintain the overall cell capacitance to bit line capacitance ratio. In the past, efforts to maintain the cell capacitance to bit line capacitance ratio have been made by segmenting the bit line array and by adding more N-sense amps, P-sense amps, and/or more column decodes. While such additional structure makes progress toward maintenance of the cell capacitance to bit line capacitance ratio, these gains are made at a cost of adding expensive overhead to the memory chip. as well as reducing the efficiency of the memory chip.

While such additional structure makes progress toward maintenance of the cell capacitance to bit line capacitance ratio, these gains are made at a cost of adding expensive overhead to the memory chip, as well as reducing the efficiency of the memory chip. In addition to the foregoing problems in the prior art, a need exists to improve yield by providing redundant memory array

structure components to replace defective memory array structure components. Defects can occur in a variety of ways, such as a foreign particle falling onto a die. It would be an advance in the art to electrically isolate such a defective memory array structure component while replacing the defective component with a properly redundant identical component, as opposed to discarding the entire memory structure.

In addition to the foregoing problems in the prior art, a need exists to improve the temporary data storage capability of high density memory array structures so as to increase the efficiency of data storage without increasing circuitry overhead for such temporary data storage.

Summary of the Invention

An object of the invention is to reduce overall power consumption of a memory structure. By reducing the overall bit line capacitance of the memory structure, less power is consumed by the memory structure for a given cell capacitance. The strength of the signal from a bit line is proportional to its capacitance. Where a bit line capacitance is smaller, the signal is stronger. The benefit of a stronger signal is a better signal-to-noise ratio. In a favorable signal-to-noise ratio there is a margin to be operational in extremes of temperature and voltage to ensure a high operational standard of the memory structure.

Another object of the invention is, for a given bit line capacitance, reducing the die size of the memory structure as compared to conventional memory structures. Reducing the die size of the memory structure furthers the objective of miniaturizing the memory structure.

A still further object of the invention is to achieve the foregoing objects while improving the temporary data storage capability of high density memory array structures so as to increase the efficiency of data storage without increasing circuitry overhead for such temporary data storage that can be rapidly accessed. A further object of the invention is to achieve the foregoing objects while improving yield by providing redundant memory array structure components to replace defective memory array structure components.

In the inventive memory structure, a plurality of memory cells are connected hierarchically below a subarray bit line. At least one subarray bit line is connected hierarchically underneath a global bit line. Each global bit line is connected to both sense amp and column decode circuitry.

Preferably, the inventive design electrically isolates subarray bit lines one from another and from the global bit line. Once a selected subarray bit line is connected to the global bit line, the global bit line is connected to only the non-isolated subarray bit line. This, in turn, reduces the overall capacitance of the bit line because only the capacitance of non-isolated subarray bit lines is added to the overall capacitance of the corresponding global array bit line that is hierarchically thereabove. Further efficiencies are achieved by the sharing of sense amp and column decode devices with multiple global bit lines and subarray bit lines. In one preferred embodiment, a single column decode and dual sense amp devices are shared by two global bit lines, there being a total of 4,096 global bit lines to make up a 4 megabit memory chip.

The inventive memory structure increases memory array efficiency in high density memories by reducing die size for a given cell capacitance to bit line capacitance ratio as compared to conventional memory structures for like bit line capacitance, or alternatively, by reducing power consumption for a higher cell to bit line capacitance ratio. The inventive memory structure can be used on a great variety of memory types, including DRAM, SRAM, flash memory, EPROM, electrical memory structures, and other types of memories.

To optimize the cell capacitance to bit line capacitance ratio, an optimum combination of subarray bit lines can be layered hierarchically underneath global bit lines. By so optimizing, overhead is reduced due to shared use of sense amps and column decode devices by the global bit lines to produce a smaller die size requirement.

The inventive memory structure scheme of subarray bit lines and global bit lines also allows for shared column decode devices to reduce die size. Gains related to reduced die size requirements are achieved, as

compared to like bit line capacitance in conventional memory structures by the sharing of sense amp and column decode devices.

The inventive memory structure also provides for refreshable data to be left floating in temporary storage on in the sense amp devices, the global array bit lines, the electrically isolatable subarray bit lines, and the memory cells which have sufficient capacitance to maintain data in temporary storage. The temporarily stored data can be rapidly accessed.

The inventive memory structure also provides for redundant global bit lines to replace defective global bit lines, provides redundant subarray bit lines to replace defective subarray bit lines, and provides redundant word lines to replace defective word lines, where the redundant subarray bit lines have identical memory cell and word line components associated therewith as the defective subarray bit lines that they replace.

After a defective memory array structure component is detected using conventional means, a redundancy logic controller deactivates or omits activating the defective memory array structure component while reassigning therefore a redundant memory array structure component. The reassignment of the redundant memory array structure component is a repair operation logically effected by overhead circuitry that can be accomplished through conventional techniques, such as laser fusing of leads to memory array structure components. The redundancy logic controller controls both column and row redundancy in the inventive memory array structure.

These and other objects and features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

Brief Description of the Drawings

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to a specific embodiment thereof which is illustrated in the

appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 shows a schematic diagram of a preferred embodiment of the inventive memory array structure as a 4 megabit memory chip having 2,048 columns, each having global bit lines on opposite sides of dual sense amp and column decode circuitry, and also shows multiple redundant columns serving as replacement components for memory array structure components in the 2,048 columns hierarchically thereover.

Figure 2 is an enlarged partial schematic diagram of the inventive memory structure seen in Figure 1 taken along the 1-1 section line, and particularly shows schematic details of the devices for the connection of two global bit lines, each global bit line being associated by eight contacts with 16 subarray bit lines, and each subarray bit line being associated with 64 word lines.

Figure 3 shows an enlarged partial schematic diagram of the memory structure seen in Figure 2 taken along the 3-3 section line, and particularly shows the area of the memory structure having two word lines and their associated subarray bit lines.

Figure 4 is an overview of a preferred embodiment of the inventive memory structure in Figure 2 taken during the 4-4 section line, which is shifted from the 3-3 section line, and shows a subarray bit line making contact with N^+ active regions, each of which is associated with a word line, which subarray bit line is paralleled both above and below by a global bit line.

Figure 5 shows a prior art memory structure in which 5 bit lines are in contact with five word lines.

Figure 6 is a cross-section side elevational view of a portion of a preferred embodiment of the inventive memory structure showing a subarray bit line making a vertically oriented contact with an N^+ active region on opposite sides of four word lines, each pair of word lines having a capacitor

region therebetween, and some word lines have an N+ active area on each side thereof, where those word lines and the dual N+ active areas on opposite sides thereof form a transistor.

Figure 7 is an overview of a preferred embodiment of the inventive memory structure showing subarray bit lines, and also showing global bit lines each of which makes contact with two N+ active areas in between the start of one subarray bit line and the end of another subarray bit line.

Figure 8 shows a schematic diagram of another preferred embodiment of the inventive memory array structure as a 16 megabit memory chip having 2,048 columns, each having super-global bit lines on opposite sides of dual sense amp and column decode circuitry, and also shows multiple redundant columns serving as replacement components for memory array structure components in the 2,048 columns hierarchically thereover.

Detailed Description of the Invention

Figure 1 shows a schematic diagram of a preferred embodiment of the inventive memory structure. While two global bit lines share a column decode device on each of 2,048 columns, there is a separate sense amp device for each global bit line. The purpose of the sense amp device connected to the global bit lines is to amplify signals on subarray bit lines connected to the global bit lines. The schematic on the left, or secondary, side of the dual sense amp and column decode circuitry is a mirror image of that on the right, or primary, side. The top global bit lines on the first column are, from left to right, GBL1000 and GBL0000. The last global bit lines are, from left to right, GBL 12047 and GBL 02047. This referencing convention shows that there are a total of 4,096 global bit lines in the memory structure shown in Figure 1.

In the preferred embodiment shown in Figure 1, each global bit lines has eight contacts to its corresponding subarray bit lines which are situated hierarchically under the global bit line. The contacts between each global bit lines and its corresponding subarray bit lines are labeled from K00 through K07. Each contact to the global bit lines connects two subarray bit lines.

Figure 1 shows a plurality of FETs, each of which has a gate and first and second electrodes, which electrodes function as source or drain regions. Each subarray bit line connects to 64 subarray FETs at a first electrode of each of the 64 subarray FETs. A second electrode of each of the 64 subarray FETs connects to a one-bit capacitor. The gate of each subarray FET in turn is connected to a word line. Through the subarray FET, each subarray bit lines is connected hierarchically above 64 word lines. Thus, each global bit lines is hierarchically above 16 subarray bit lines and each subarray bit lines is hierarchically above 64 word lines, such that the schematic of Figure 1 shows four megabits of 4,194,304 bits of memory. These four megabits are made up by 2,048 columns, each column having two global bit lines, each global bit lines having 16 electrically violatable subarray bit lines having subarray FETs connected to 64 word lines. Figure 2 is an enlarged view of the upper quadrant of the primary side of Figure 1 shown from the 2-2 section line seen on the schematic diagram of Figure 1. Figure 2 shows global bit lines GBL00000 connecting to contact K00 through K07. Global bit lines GBL00000 is stacked over subarray bit lines SABL00 through SABL07. By way of example of the subarray structure, subarray bit lines SABL00 is connected to global bit lines GBL00000 through contact K00. Contact K00 connects to subarray bit lines SABL00 through FET controller BLK00. Subarray bit lines SABL00 has an equilibrate controller FET shown as EQBP00. The equilibration devices, seen in Figures 1 and 2 have EQBP00, EQBP01, etc. are shown as FETs. However, such an equilibration device can be substituted for circuitry in the sense amp devices.

With respect to Figure 1, for both the primary and secondary sides, each sense amp device the ability to store the signal of the global bit line when electrically isolated from the corresponding global bit line. Each sense amp device represents, by way of example and illustration, a means for sensing and amplifying the signal on the corresponding global bit line, and for outputting an amplified global bit line signal to a corresponding column decode device. The means for sensing and amplifying the global bit line signal is electrically isolated by a means for electrical switching situated in

the means for sensing and amplifying the global bit signal. Here, the column decode device represents, by way of example and illustration, a means for decoding the amplified global bit line signal.

Each global bit line has a capacitance to store the global bit line signal when electrically isolated from the corresponding sense amp device, and from its corresponding subarray bit lines. Like the electrical isolation of the global bit line, each subarray bit line has a capacitance to store a subarray bit line signal when electrically isolated from its corresponding global bit line, and from the corresponding plurality of memory cells or capacitors associated therewith. Lastly, each memory cell or capacitor has a capacitance to store a storage signal when electrically isolated from its corresponding subarray bit line.

In order to effect the foregoing electrical isolation scheme, the inventive integrated memory array circuit in Figure 1 isolates the sense amp device by incorporating therein a means for electrical switching, which is represented and illustrated by the sense amp devices seen in Figure 1. The global bit line is electrically isolated by both the electrical switching means and by the FETs or access devices corresponding to the global bit line. Each subarray bit line is electrically isolated by a corresponding one of the access devices hierarchically thereover, and by its corresponding subarray access devices hierarchically thereunder. Finally, each memory cell or capacitor is electrically isolated by a corresponding subarray access device or FET. When the foregoing memory array structure components of Figure 1 have been electrically isolated, the data temporarily stored therein can be readily and rapidly accessed.

Figure 2 is an enlarged view of the upper quadrant of the primary side of Figure 1 shown from the 2-2 section line seen on the schematic diagram of Figure 1. Figure 2 shows global bit line GBL00000 connecting to contacts K00 through K07. Global bit line GBL00000 is stacked over subarray bit line SABL00 through SBL07. By way of example of the subarray structure, subarray bit line SABL00 is connected to global bit line GBL00000 through contact K00. Contact K00 connects to subarray bit line SABL00 through FET

controller BLK00. Subarray bit line SABL00 has an equilibrate controller FET shown as EQBP00. The equilibration devices, seen in Figures 1 and 2 have EQBP00, EQBP01, etc. are shown as FETs. However, such an equilibration device can be substituted for circuitry in the sense amp devices.

Through a first electrode of a subarray FETs, subarray bit line SABL00 connects to word lines WL00 through WL63 which are connected, respectively, to the gates of the subarray FETs. Word lines WL00-WL63 are respectively connected through the gate of subarray FETs Q00 through 63 to a first electrode of FETs Q00 through Q63 all of which are connected to subarray bit line SABL00. Each word line WL00 through WL63 is associated, respectively, to capacitors C00 through C63, via the gate of subarray FETs Q00 through Q63. Each capacitor C00 through C63 serves as an example and illustration of a means for storing and communicating a storage signal. The capacitor opposite the subarray bit line SABL00 shows connection to a cell plate indicated by CP00000. The cell plate is a blanket-like structure covering most of the memory structure. Holes are positioned on the cell plate through which contact is made with N^+ active areas by the subarray bit lines.

In Figure 1, each sense amp device represents, by way of example and illustration, a means for sensing and amplifying the signal on the corresponding global bit line, and for outputting an amplified global bit line signal to a corresponding column decode device. Here, the column decode device represents, by way of example and illustration, a means for decoding the amplified global bit line signal.

Figure 1 shows a representation of a plurality of redundant columns which are generally labeled with redundant components as follows: a primary sense amp device SA02047c, a secondary sense amp device SA12047c, the primary and secondary sense amp devices sharing a redundant column decode device CD2047c, a primary global bit line GBL02047c, and a secondary global bit line GBL12047c. In the case of each reference numeral associated with the redundant memory array structure components, the "c" represents at least one redundant memory array structure component. Thus, it is

contemplated that multiple redundant columns having associated redundant components are represented by Figure 1.

Figure 1 also shows a redundancy logic controller RCL which, through conventional means, receives input as to the detection of a defective memory array structure component, and then either deactivates or omits activating the defective memory array structure component while reassigning therefore a redundant memory array structure component. By way of example, and not by way of limitation, when a primary global bit lines is detected to be defective, an unreassigned primary redundant global bit line on a redundant column is logically reassigned to take the place of the defective global bit line. When a secondary subarray bit line is detected to be defective, a secondary redundant global bit line having at least one unreassigned secondary redundant subarray bit line thereunder, a unreassigned secondary redundant subarray bit line, and a secondary redundant column hierarchically thereover are logically reassigned by logic controller RCL to take the place of the defective primary subarray bit line. Finally, when a defect is detected in a memory cell, or an access device associating a memory cell with a corresponding word line, the subarray bit line associated with the defect is either deactivated or is omitted from activation along with its associated components, and a redundant global bit line having at least one unreassigned redundant subarray bit line, an unreassigned redundant subarray bit line with its associated component memory cells and access devices, and the redundant column hierarchically thereover are all logically reassigned by logic controller RCL to take the place of the subarray bit line associated with the defect. Preferably, each of the redundant subarray bit lines hierarchically under any one redundant column is reassigned before the next redundant column is used for redundant structures hierarchically thereunder. In this way, the use of redundant components in redundant column is efficient.

Logic controller RCL represents, by way of example and illustration, a means for activating one of the subarray bit lines in a redundant column corresponding to one of the subarray bit lines in the non-redundant column. Logic controller RCL also represents, by way of example and illustration, a

means of storing addresses of the activated one of the redundant subarray bit lines.

The benefit realized by the redundancy aspect of the inventive memory array structure is that the failure of a memory cell, access device, subarray bit line, or sense amp device, does not require that an entire column be discarded as unusable. For example, when a primary global bit line on the primary side of a column is defective, the column decode device and the secondary side of the column, assuming no defects in the secondary global bit line thereof, are still usable. By preserving as much of each column in the hierarchy thereof that is non-defective, yield in manufacturing is improved so as to realize cost savings through lower rejection rates.

The cell plate and each global bit line are connected to a separate sense amp device. As shown in Figure 2, global bit lines GBL00000 and GBL00001 are connected, respectively, to sense amp devices SA00000 and SA00001. Column decode devices CD0000 and CD00001 are associated, respectively, with global bit lines GBL00000 and GBL00001. Each column decode device interfaces with dual sense amp devices. Thus, an efficient use of the global bit lines exists through sharing of sense amp and column decode circuitry to interface with the word lines of multiple subarray bit lines.

Each word line is in electrical communication with a corresponding word line in each of the 2,048 columns seen in Figure 1. Thus, there are 2,047 other word lines in electrical communication with each word line. The electrical communication between word lines, while not seen in Figure 1 and 2, is accomplished by interconnections between each gate of each subarray FET associated with the corresponding word lines. As seen in Figure 2, the subarray FETs associated with the word lines are Q00 through Q63 for each subarray bit line. By way of illustration of such correspondence of word line interconnection, each gate of each subarray FET Q00 of each subarray bit line SABL00 of global bit lines GBL00000 through GBL02047 are electrical connected together. Similar interconnection conventions apply for the gates of subarray FETs Q01 through Q63 in each of the 2,048 columns seen in Figure 1.

While Figures 1 and 2 depict a shared column decode device between sense amp devices, it is also contemplated that the column decode device need not be shared by sense amp devices. It is contemplated within the scope of the present invention that a column decode device can be separated from both the sense amp devices and global bit lines.

Figure 3 is an enlarged sectional view of the schematic diagram of Figure 2 shown along the 3-3 section line of Figure 2. In Figure 3, word lines WL13 and WL14 are shown, respectively, by connection to the gate of subarray FETs Q13 and Q14, which are respectively associated with capacitors C13 and C14. Subarray bit line SABL00 is hierarchically above subarray FETs Q13 and Q14 through connection to a first electrode of subarray FETs Q13 and Q14. SABL00 is stacked below global bit line GBL00000. Figure 3 schematically depicts two of the 64 word lines associated with subarray bit line SABL00.

Figure 4 shows a partial and enlarged layout of a preferred embodiment of the inventive memory structure seen in Figure 2 along the 4-4 section line in which there are pictured two global bit lines, one subarray bit line, and eight word lines. The global bit line and the subarray bit line are seen on a single layer of conductive material. Figure 4 is shown with several layers removed for simplicity. Subarray bit line SABL00 is stacked in between global bit lines GBL00000 and GBL00001. Running perpendicularly to subarray bit line SABL00 are word lines WL12 through WL19. Subarray bit line SABL00 connects to an N^+ active area associated with a word line at each "X" seen in Figure 4. Neither of the two global bit lines seen in Figure 4 are connected to an N^+ active area. Word lines WL12 through WL19 are preferably composed of polysilicon. It is preferable that each global bit line and subarray bit line is made of a electrically conductive material, such as a metal.

Because of the staggering of the layout diagram depicted in Figure 4, there is the appearance that only two word lines are situated in between contacts with subarray bit line SABL00. However, without the depicted staggering view seen in Figure 4, four word lines would be seen between each

contact with subarray bit line SABL00, as to be described with respect to Figure 6 hereinafter.

In an alternative embodiment of the inventive memory structure not seen in Figure 4, the global bit line and the subarray bit line are on separate conductive layers, such as separate metal layers, and an oxide layer separates the conductive layer of the global bit line from the conductive layer of the subarray bit line.

Figure 5 depicts a prior art memory array structure where no subarray bit lines are featured. Rather, each bit line BL00 through BL04 contacts each word line WL12 through WL16. The place of contact is seen by an "X" on Figure 5 where each bit line BL00 through BL04 makes contact with an N^+ active area associated with a word line WL12 through WL16. As can be seen in Figure 5, there are four word lines in between each point of contact with each bit line.

Figure 6 shows a cross-sectional side elevational view of a preferred embodiment of the inventive memory structure, where four word lines are situated between two contacts with a subarray bit line, which contacts are also electrically connected to an N^+ active area. While Figure 6 shows only a portion of a preferred embodiment of the inventive memory structure, the layered nature of the structure is that metallic bit lines are disposed over a layer of BPSG. The layer of BPSG is disposed over a polysilicon layer of top cell plate which covers over a layer of cell dielectric. Under the layer of cell dielectric is a series of polysilicon storage nodes. Each storage node connects with a buried contact which connects to an N^+ active area forming a fragmented bottom layer of the memory structure. Polysilicon word lines are positioned in between the buried contacts and the N^+ active areas. Contact fill segments extend through the layer of BPSG, the layer of top cell plate, the cell dielectric layer, around the storage nodes, around the buried contacts, and around the word lines so as to form a contact from the bit lines to the N^+ active areas.

A portion of the inventive memory array structure is generally shown at 10 in Figure 6. A subarray bit line 12 is seen as being situated on the

same conductive layer with a global bit line 11 shown in phantom. In an alternative embodiment not shown, a global bit line 13 can be stacked above subarray bit line 12 on a separate conductive layer. Word lines 14, 16, 18, 20 are seen positioned between a pair of contact fills 22 and 24.

N^+ active regions are shown at reference numeral 30. A capacitor is illustrated as a cell dielectric 36 surrounded by a top cell plate 36 and storage node 34. A field oxide is seen at 40, and oxides are seen at 42, 44, and 46. A layer of BPSG 48 is situated between contact fills 22, 24. A barrier 50 is immediately below subarray bit line 12. A layer of nitride passivation 52 is situated above oxide layer 46.

A transistor is made up by two N^+ active areas on either side of word lines 14, 16, 18 and 20 which are preferably polysilicon word lines. A capacitor, composed of storage node 34 having cell dielectric 36 that is covered over by top cell plate 38, is seen on the right side of each word line and immediately above each N^+ active area.

Figure 7 is a depiction of the areas of contact between a global bit line and its corresponding subarray bit lines. Contact areas K-0, K-1, and K-2 are contacts, respectively, from global bit lines GBL-0, GBL-1 and GBL-2 to N^+ active areas associated with subarray bit lines that correspond, respectively to FETs BLK0-01, BLK0-00, BLK1-01, BLK1-00, BLK2-01, and BLK2-00. Each contact K-0, K-1, and K-2 has two corresponding FETs. Global bit line GBL-0 has corresponding FETs BLK0-01 and BLK0-00. Contact K-1 associated with global bit line GBL-1 has corresponding FETs BLK1-01 and BLK1-00. Contact K-2 associated with global bit line GBL-2 has corresponding FETs BLK2-01 and BLK2-00.

A gate is depicted for each of the six FETs BLK0-00, BLK0-01, BLK1-00, BLK1-01, BLK2-01, and BLK2-00. By way of example, FET BLK0-00 has gate GAT-0 associated therewith, FET BLK1-00 has gate GAT-1 associated therewith, and FET BLK2-00 has gate GAT-2 associated therewith. The contacts K-0, K-1, and K-2 with their corresponding FETs establish connection between global bit lines and the subarray bit lines hierarchically thereunder. In Figure 7, both the subarray bit lines and the

global bit lines are on the same conductive layer. In other preferred embodiments of the inventive memory array structure, the subarray bit lines and the global bit lines can be on different conductive layers.

An advantage gained by the invention, which advantage can be understood by the example of the circuitry depicted in Figures 4 and 7, is that subarray bit lines are electrically isolated at a constant voltage while the global bit line therebetween is operational. In so doing, the voltage of the global bit line is not effected by with the two subarray bit lines that are adjacent to the global bit line, and the bit line coupling component between adjacent bit lines is not hindered. By holding subarray bit line voltage constant, the effect of bit line coupling capacitance is reduced, as compared to conventional bit line structures where voltage is not held constant on adjacent bit lines. Thus, the electrical isolation of subarray bit lines that are adjacent to a global bit line prevents interference with the voltage on the global bit line.

The inventive memory structure electrically isolates subarrays from causing a moving effect upon the voltage of a corresponding global bit line. This electrical isolation is effected by connecting only a selected subarray bit line, and its associated memory cells, to a global bit line at a time. Unlike conventional memory structures which connects all memory cells to the bit lines simultaneously, the inventive memory array structure permits that only some of the memory cells are connected to a global bit line through access devices associated with a select subarray bit line at a time.

Electrical isolation of the subarray bit lines adjacent to a global bit line acts to block capacitance interference with the global bit line and reduces the noise effect of bit line coupling components known to conventional memory structures lacking such adjacent bit line isolation. As can be seen in Figures 4 and 7, the interleaving of electrically isolated subarray bit lines with global bit lines, where the global bit lines does not contact the N^+ active area except at periodic points of contacts, enables an electrical blocking effect due to the electrical isolation of the subarray bit line adjacent to a global bit line.

The bit line coupling component is 15% of the overall bit line capacitance between adjacent bit lines, or a total of 30% of the capacitance for a bit line having two adjacent bit lines. The inventive memory array structure, by electrically isolating subarray bit lines, effectively reduces the bit line capacitance by about 70%. The absence of an electrical barrier for adjacent bit lines in conventional memory structures is detrimental, in that conventional memory structures connect all memory cells to the bit lines simultaneously, which causes about a 70% higher bit line coupling component. By reducing the bit line coupling component by about 70% through electrical isolation of adjacent subarray bit lines in the inventive memory array structure, there is a marked improvement in the global bit line signal strength. As seen in Figures 4 and 7, the patterning of the memory structure combined with the electrical isolation of subarray bit lines adjacent to a global bit line, furthers the objective of a higher signal to noise ratio.

The isolation of subarray bit lines from global bit lines is an important factor in reducing capacitance of the memory structure because on each cycle of read or write operations these capacitors must be charged and discharged. By reducing the global bit line capacitance, there is a concomitant reduction in the power consumption. While a conventional memory structure connects all capacitors therein simultaneously, only selected capacitors are connected within the inventive memory structure. The capacitance coupling component between bit lines is much smaller due to the smaller segmenting of the connections therebetween. For each small segment of word lines activating FETs to connect selected memory cells to their corresponding global bit lines that are hierarchically connected thereover, the overall capacitance is less than conventional bit lines having all of its memory cells connected thereto simultaneously. The global bit line, once connected to a selected subarray bit line, only senses the capacitance between the immediately adjacent two subarray bit lines. Due to this isolation of subarray bit lines, the global bit line does not sense the isolated and unconnected subarray bit lines so that the overall capacitance of the global bit line is reduced.

For a given bit line capacitance, the die size of the memory structure is smaller than conventional memory structures because in the inventive structure sense amp and column decode devices are shared by or among more memory cells, thus using less overhead circuitry.

Another preferred embodiment of the invention is shown in Figure 8 where, by way of example, a super-global bit line SGBL00000 is hierarchically above four global bit lines GBL0, GBL1, GBL2, GBL3 through four FETs SBLK00, SBLK01, SBLK02, SBLK03. Each global bit line can be electrically isolated from its corresponding super-global bit line similar to the electrical isolation of subarray bit lines from adjacent global bit lines as is described herein with respect to Figures 1-4, 6 and 7. One global bit line is interfaced through a FET associated between the unisolated global bit line and its corresponding super-global bit line.

In Figure 8, there are 2,048 columns, each column having two super-global bit lines connecting to dual sense amp devices which in turn share a column decode device. Each of the two super-global bit lines have four contacts to four global bit lines, which contacts are similar to those described herein with respect to Figure 4. As in Figures 1 and 2 and text herein associated therewith, each global line in the alternative preferred embodiment has 8 contacts to 16 subarray bit lines. Correspondingly, each subarray bit line has contacts to 64 word lines through a first electrode of each of 64 subarray FETs. Additionally, each word line actives through a subarray FET gate to connect a second electrode of the 64 subarray FETs to a means for storing a one bit charge, such as a capacitor. In such an embodiment of the invention, a 16 megabit memory array is accomplished.

While super-global bit lines and global bit lines are intended to be connected through FET devices, the number of global bit lines to be connected through FETs to a super-global bit line is contemplated to vary within the scope of the invention. Additionally, the super-global bit line is contemplated to be on a different conductive layer than the global lines associated therewith, where the subarray bit lines and the global bit lines can be on the same or on different conductive layers. Thus, embodiments of the

inventive memory array structure incorporating super-global bit lines can have two or three conductive layers for the super-global bit lines, the global bit lines, and the subarray bit lines.

With respect to Figure 8, for both the primary and secondary sides, each sense amp device has the ability to store the signal of the super-global bit line when electrically isolated from the corresponding super-global bit line. Similarly, each super-global bit line has a capacitance to store the super-global bit line signal when electrically isolated from the corresponding sense amp device, and from its corresponding global bit lines. Similarly, each global bit line has the having a capacitance to store the super-global bit line signal when electrically isolated from the super-global bit line, and from its corresponding plurality of subarray bit lines. Like the electrical isolation of each global bit line, each subarray bit line has a capacitance to store a subarray bit line signal when electrically isolated from its corresponding global bit line, and from the corresponding plurality of memory cells or capacitors associated therewith. Lastly, each memory cell or capacitor has a capacitance to store a storage signal when electrically isolated from its corresponding subarray bit line.

In order to effect the foregoing electrical isolation scheme, the inventive integrated memory array circuit in Figure 8 isolates the sense amp device by incorporating therein a means for electrical switching, which is represented and illustrated by the sense amp devices seen in Figure 8. The super-global bit line is electrically isolated by the electrical switching means of the corresponding sense amp device, and by the global access devices or the global FETs. Similarly, each global bit line is electrically isolated by a corresponding one of the global access devices or FETs, and by the access devices corresponding thereto. Each subarray bit line is electrically isolated by a corresponding one of the access devices hierarchically thereover, and by its corresponding subarray access devices hierarchically thereunder. Finally, each memory cell or capacitor is electrically isolated by a corresponding subarray access device or FET. When the foregoing memory array structure components of Figure 8 have been electrically isolated, the data temporarily stored therein can be readily and rapidly accessed.

Figure 8 also depicts a redundancy schematic having a scheme that functions similarly to the redundancy scheme of Figure 1. In Figure 8, there is shown a representation of a plurality of redundant columns which are generally labeled with redundant components as follows: a primary sense amp device SA02047c, a secondary sense amp device SA12047c, the primary and secondary sense amp devices sharing a redundant column decode device CD2047c, a primary super-global bit line SGBL02047c, and a secondary super-global bit line SGBL12047c. In the case of each reference numeral associated with the redundant memory array structure components, the "c" represents at least one redundant memory array structure component. Thus, it is contemplated that multiple redundant columns having associated redundant components are represented by Figure 8.

Figure 8 also shows a redundancy logic controller RCL which, through conventional means, receives input as to the detection of a defective memory array structure component, and then either deactivates or omits activating the defective memory array structure component, while reassigning therefore a redundant memory array structure component. By way of example, and not by way of limitation, when a secondary super-global bit line SGBL00001 is detected to be defective, a redundant secondary super-global bit line SGBL02048 on redundant column 2049 is logically reassigned to take the place of defective secondary super-global bit line SGBL00001. Similarly, when a primary global bit line is detected to be defective, a redundant primary super-global bit line having at least one unreassigned primary redundant global bit line, and an unreassigned primary global bit line on a redundant column hierarchically thereover are logically reassigned to take the place of the defective global bit line. When a subarray bit line is detected to be defective, an unreassigned redundant subarray bit line, a redundant global bit line hierarchically thereover, and a redundant super-global bit line on a redundant column are all logically reassigned by logic controller RCL to take the place of the defective subarray bit line. Finally, when a defect is detected in a memory cell, or an access device associating a memory cell with a corresponding word line, the subarray bit line associated with the defect is

either deactivated or is omitted from activation along with all memory cells and access devices associated therewith, and an unreassigned redundant subarray bit line with its corresponding memory cells and access devices, a redundant global bit line hierarchically thereover, and a redundant super-global bit line hierarchically thereover on a redundant column are all logically reassigned by logic controller RCL to take the place of the subarray bit line associated with the defect. Preferably, each of the redundant subarray bit lines hierarchically under any one redundant column is reassigned before the next redundant column is used for reassigning memory components thereunder. In this way, the use of redundant components in each redundant column is efficient.

The inventive memory array structure is contemplated to be used in a variety of memory types, each of which incorporates a plurality of access devices into the memory array structure of the memory type. The access devices are FETs in a DRAM embodiment, an example of which is a subarray FET that is activated by a word line signal from a word line to connect a capacitor to a subarray bit line through the subarray FET, and where other FETs selectively isolate or connect the subarray bit lines to global bit lines. In the case of SRAM, the access devices may be two FETs. In the case of flash memory, each access device may have a transistor with a floating gate while the memory cell forms a part of the access device itself.

For each memory type, the function of the access device is to serve as an electrical switch. As an electrical switch, each access device is capable of electrically isolating lines or devices that are connected to the access device. Alternatively, the access device is capable of electrically communicating a signal between lines or devices that are connected to the access device. Thus, access devices are capable of electrically isolating subarray bit lines from a corresponding global bit line, and electrically isolating both word lines and corresponding storing and communicating means.

In a still further preferred embodiment of the invention, which also can be seen in both Figures 1 and 8, it is contemplated that each subarray bit line has allocated some of the capacitors and subarray FETs to be redundant and

has allocated the other capacitors and subarray FETs to be non-redundant and replaceable if defective by those that are redundant. By way of example of the 64 component sets on each subarray bit line, thirty-two of the capacitors, subarray FETs, and word lines are memory array structure components, while the other thirty-two of the capacitors, subarray FETs, and word lines are placement memory array structure components. Thus, if one word line in the main thirty-two word lines becomes defective, a replacement word line, subarray FET, and associated capacitor is assigned to replace this defect within the same subarray bit line in the same column so as to repair the word line in that column. In this embodiment of the invention, each word line is in electrical communication with a row decode driver device, which is represented by redundancy logic controller RCL. Redundancy logic controller RCL also represents both logic and hardware circuitry to repair the defective word line by reassigning a redundant word line and associated redundant capacitor in the same subarray bit line and the same column. Through conventional means, redundancy logic controller RCL receives input as to the detection of a defective word line, and then either deactivates or omits activating the defective word line while reassigning therefore a redundant word line and associated redundant capacitor. Thus, redundancy logic controller RCL performs the function of effecting repairs to the inventive memory array structure by controlling column redundancy, row redundancy, or both column and row redundancy.

In yet a further preferred embodiment of the invention, replacement subarray bit lines with associated replacement access devices and replacement memory cells are provided in the same side of the column to replace defective subarray bit lines and associated components within the same column. These replacement components within the same column can be combined with the column and row redundancy structures described above. In each of such embodiments of the invention, the redundancy logic controller controls the replacement of defective components and the storage of memory addresses necessary to logically effect such replacement.

In summary, for a fixed bit line capacitance the inventive memory structure is smaller in die size than convention memory structure die sizes by the provision of the inventive subarray bit lines structure with shared column decode devices between dual sense amps. Alternatively, by providing a plurality of word lines for each subarray bit line, and electrically isolatable subarray bit lines for each global bit line via access devices, a reduced effect on bit line capacitance is realized because the bit line capacitance component is reduced by connecting only selected memory cells at any one time. As the bit line capacitance component is reduced, there will also be a reduced power consumption for the memory structure because less power is needed to charge the unisolated parts of the memory array structure.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrated and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed is:

1. An integrated memory device comprising:

a global bit line;

a plurality of subarray bit lines;

a plurality of addressable subarray bit line access devices connected to the global bit line and the plurality of subarray bit lines for selectively coupling one of the plurality of subarray bit lines to the global bit line;

a plurality of memory storage cells;

a plurality of addressable memory cell access devices connected to the plurality of memory storage cells for selectively coupling one of the plurality of memory storage cells to one of the plurality of subarray bit lines; and

a sense amplifier circuit connected to the global bit line for sensing and amplifying a voltage on the global bit line.

2. The integrated memory device of claim 1 further comprising:

an isolation device between the global bit line and the sense amplifier circuit for electrically isolating the global bit line from the sense amplifier circuit.

3. The integrated memory device of claim 1 wherein the global bit line has a capacitance capable of storing a charge.

4. The integrated memory device of claim 1 wherein the global bit line and the plurality of subarray bit lines are fabricated on a single metal layer.

5. An integrated memory device comprising:

a super-global bit line;

a plurality of global bit lines;

a plurality of subarray bit lines;

a plurality of addressable global bit line access devices connected to the super-global bit line and the plurality of global bit lines for selectively coupling one of the plurality of global bit lines to the super-global bit line;

a plurality of addressable subarray bit line access devices connected to the plurality of global bit lines and the plurality of subarray bit lines for selectively coupling one of the plurality of subarray bit lines to one of the plurality of global bit lines;

a plurality of memory storage cells;

a plurality of addressable memory cell access devices connected to the plurality of memory storage cells for selectively coupling one of the plurality of memory storage cells to one of the plurality of subarray bit lines; and

a sense amplifier circuit connected to the super-global bit line for sensing and amplifying a voltage on the super-global bit line.

6. The integrated memory device of claim 1 or claim 5 wherein the plurality of addressable subarray bit line access devices are transistors electrically connected between the global bit line and the plurality of subarray bit lines.

7. The integrated memory device of claim 1 or claim 5 wherein the plurality of memory cell access devices are transistors electrically connected between the plurality of memory storage cells and the plurality of subarray bit lines.

8. The integrated memory device of claim 1 or claim 5 wherein each of the plurality of subarray bit lines have a capacitance capable of storing a charge.

9. The integrated memory device of claim 1 or claim 5 further comprising:

a redundant global bit line;

a plurality of redundant subarray bit lines;

a plurality of redundant subarray access devices connected to the redundant global bit line and the plurality of redundant subarray bit lines for selectively coupling one of the plurality of redundant subarray bit lines to the redundant global bit line;

a plurality of redundant memory storage cells;

a plurality of redundant memory cell access devices connected to the plurality of redundant memory storage cells for selectively coupling one of the plurality of redundant memory storage cells to one of the plurality of redundant subarray bit lines;

activation circuitry connected to the plurality of redundant subarray access devices and the plurality of redundant memory cell access devices; and

a sense amplifier circuit connected to the redundant global bit line.

10. The integrated memory device of claim 5 wherein the plurality of global bit lines and the plurality of subarray bit lines are fabricated on a single metal layer.

11. A method of reading data from a memory device having a hierarchical bit line structure, the method comprising the steps of:

selectively activating one of a plurality of memory cell access devices connected between one of a plurality of memory storage cells and one of a plurality of subarray bit lines;

coupling a charge stored on the one of the plurality of memory storage cells to the one of the plurality of subarray bit lines;

selectively activating a subarray access device connected between the one of the plurality of subarray bit lines and a global bit line;

coupling a charge stored on the one of the plurality of subarray bit lines to the global bit line, thereby producing a global bit line voltage; and

sensing and amplifying the global bit line voltage.

12. The method of claim 11 further including the step of outputting the amplified global bit line voltage.

13. A method of repairing a memory device having a hierarchical bit line structure, the method comprising the steps of:

identifying a defective global bit line;

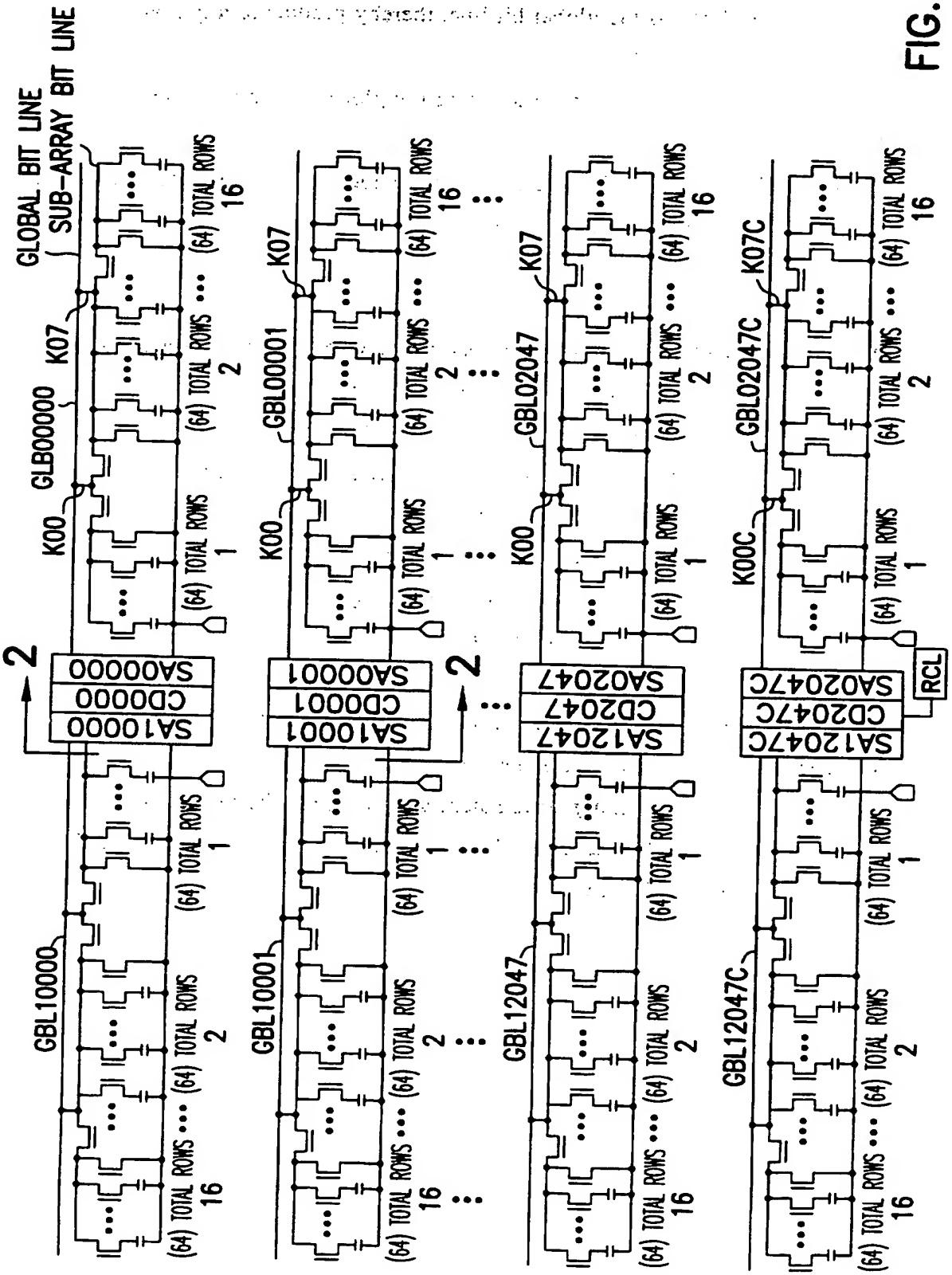
assigning a redundant global bit line to respond to an address of the defective global bit line;

identifying a defective subarray bit line; and

assigning a redundant subarray bit line to respond to an address of the defective subarray bit line.

14. The method of claim 13 wherein the step of assigning a redundant subarray bit line comprises the step of:

assigning a redundant global bit line having an unassigned redundant subarray bit line to respond to an address of the defective subarray bit line.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K07
GBL00001
K07
K00C
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GBL12047
GBL12047C
SA00000
CD0000
SA10000
SA00001
CD0001
SA10001
SA02047
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2
(64) TOTAL ROWS
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2
16

FIG. 1

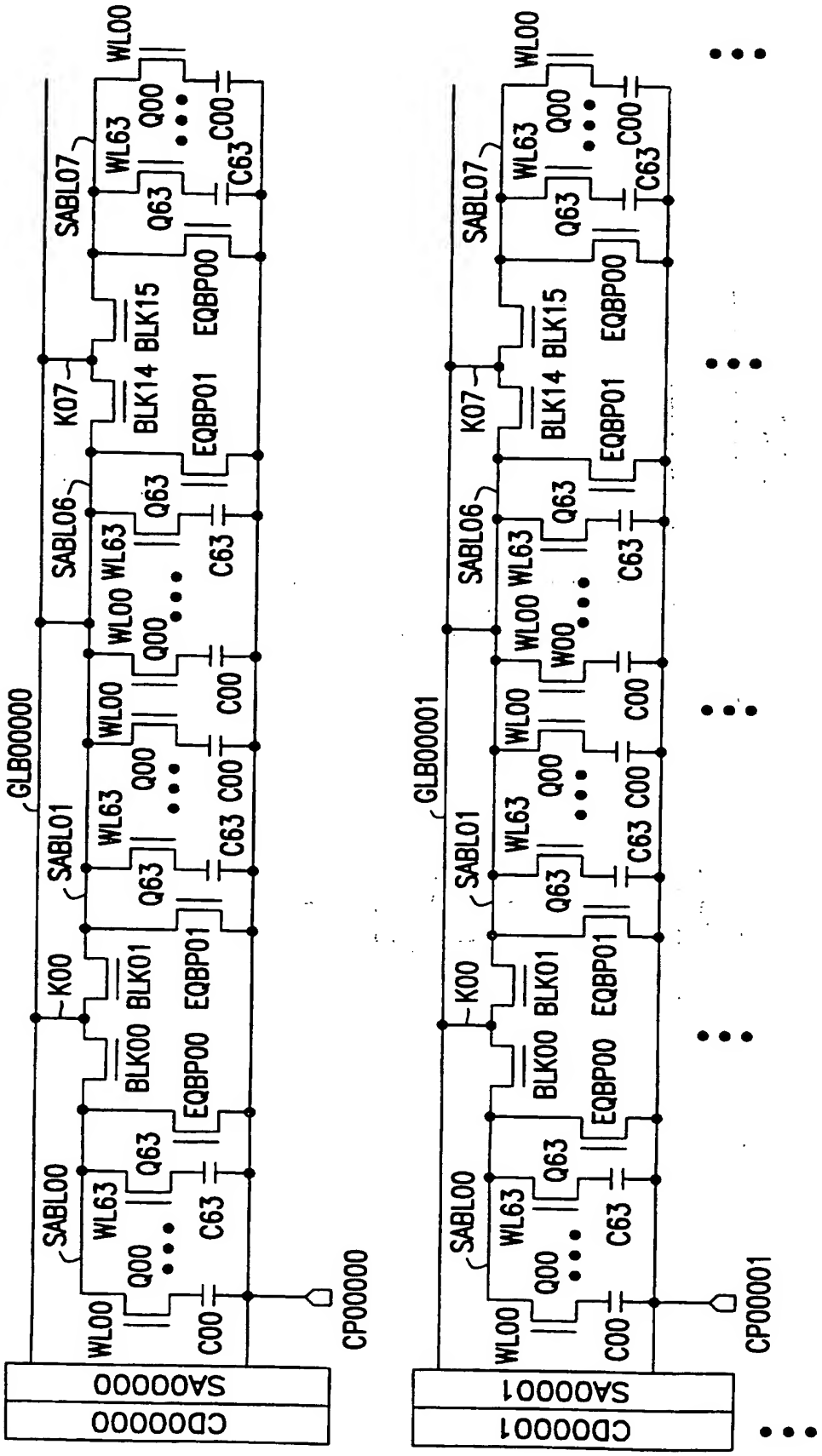
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FIG. 2

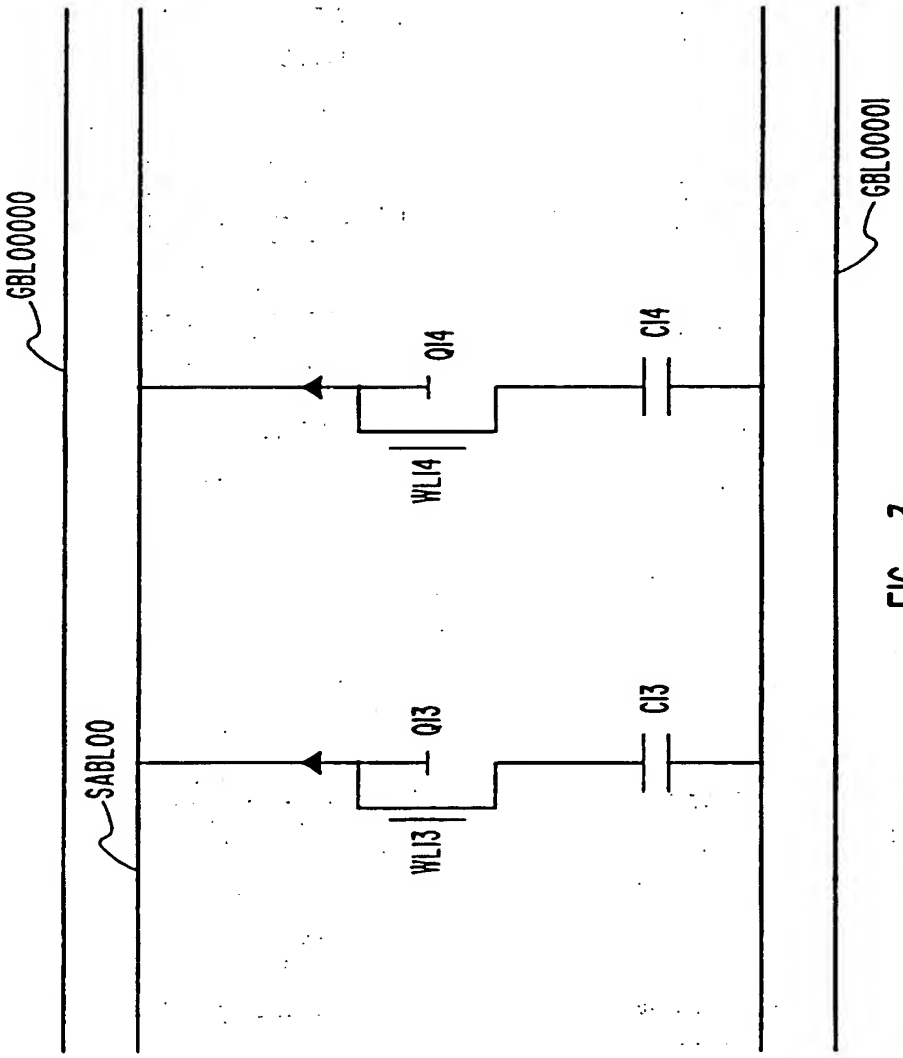

FIG. 3

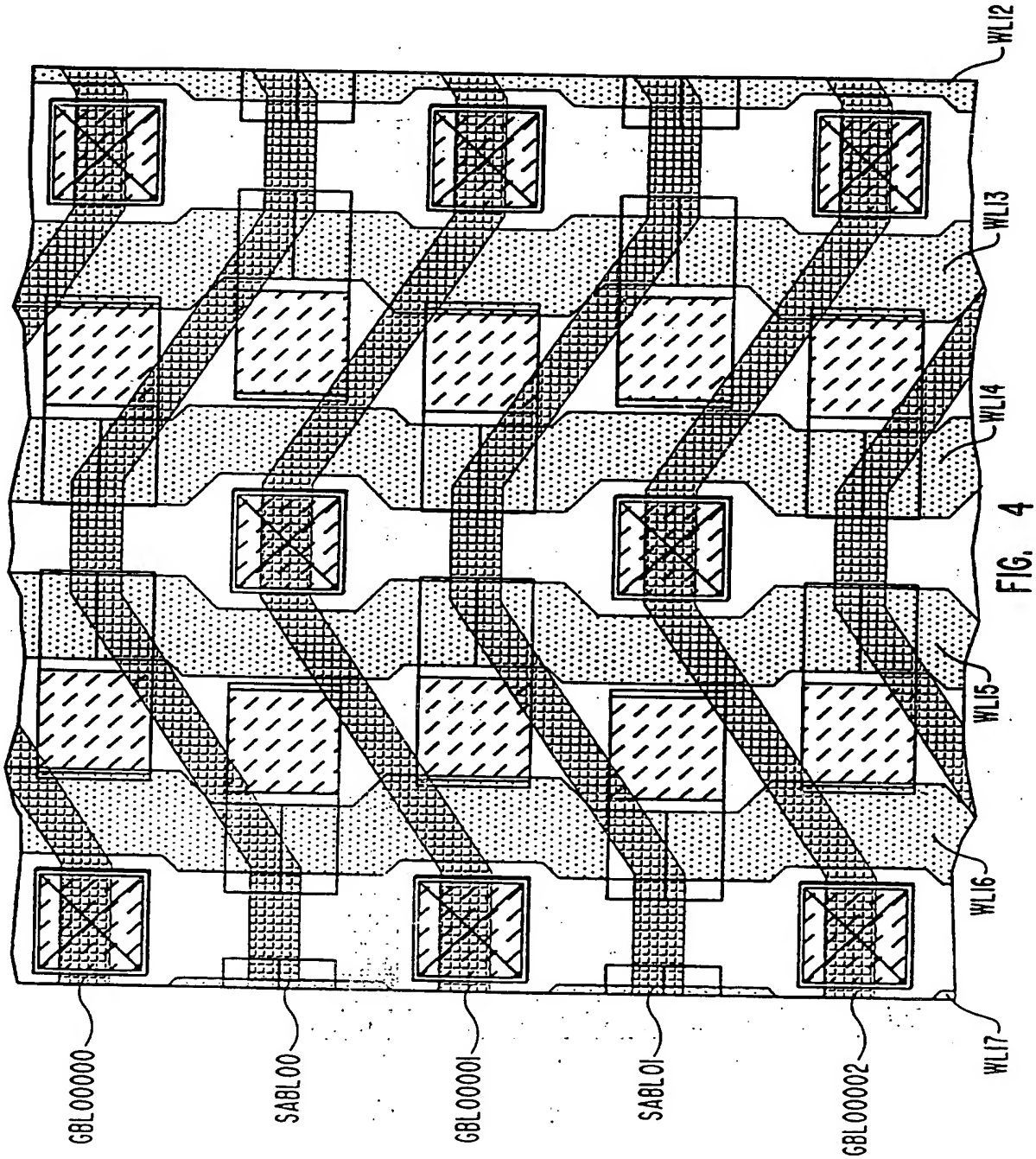
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FIG. 4

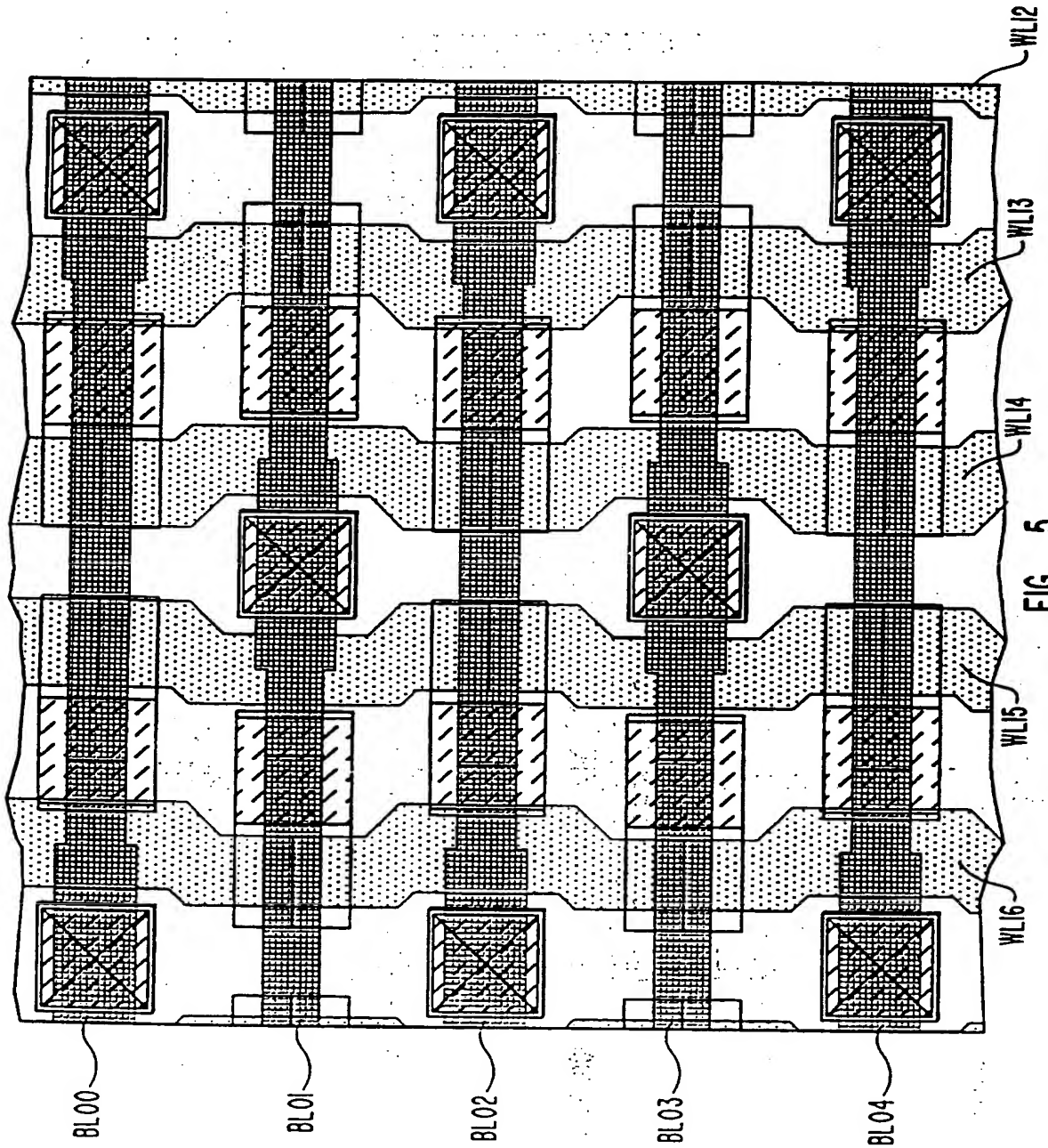

FIG. 5
(PRIOR ART)

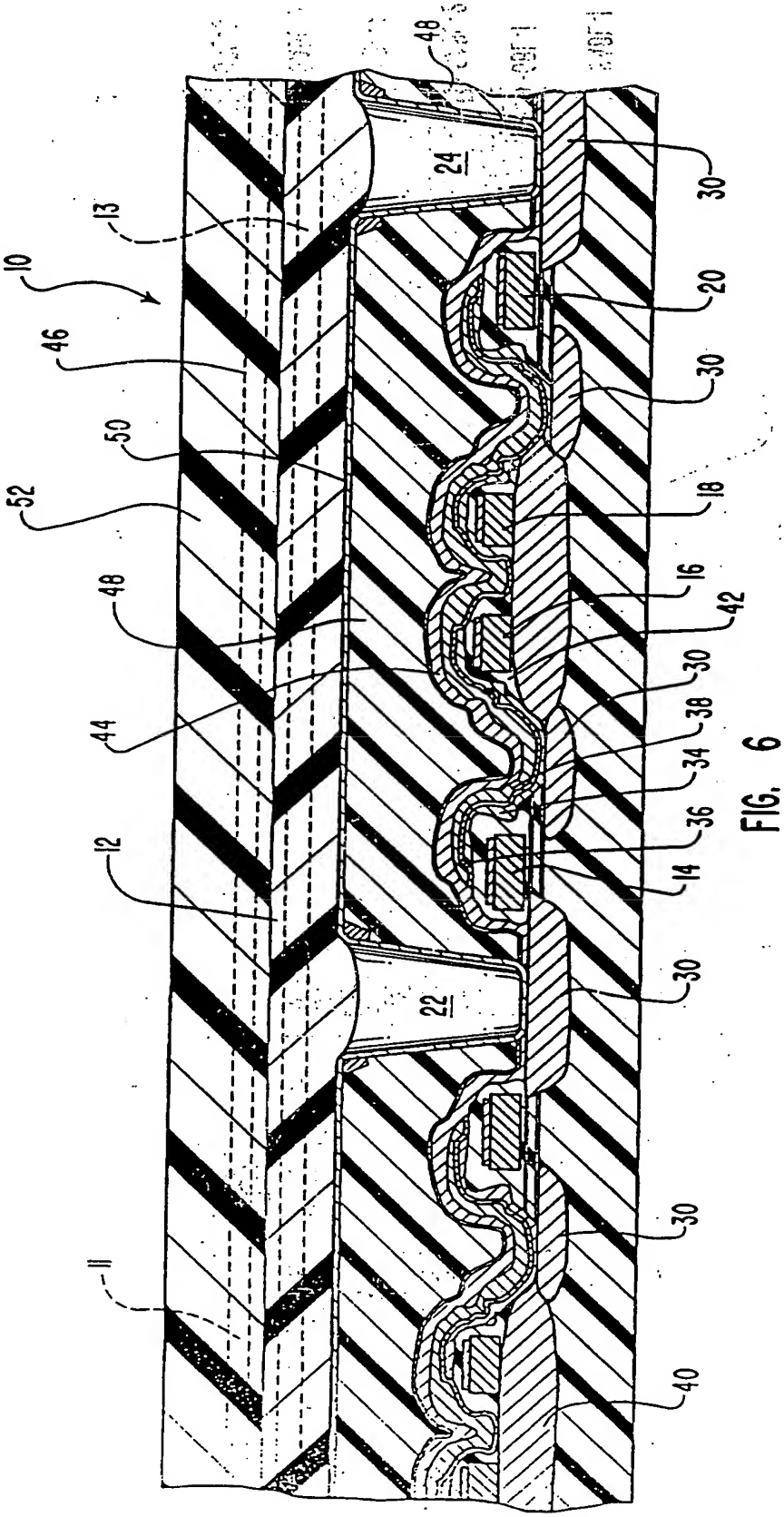
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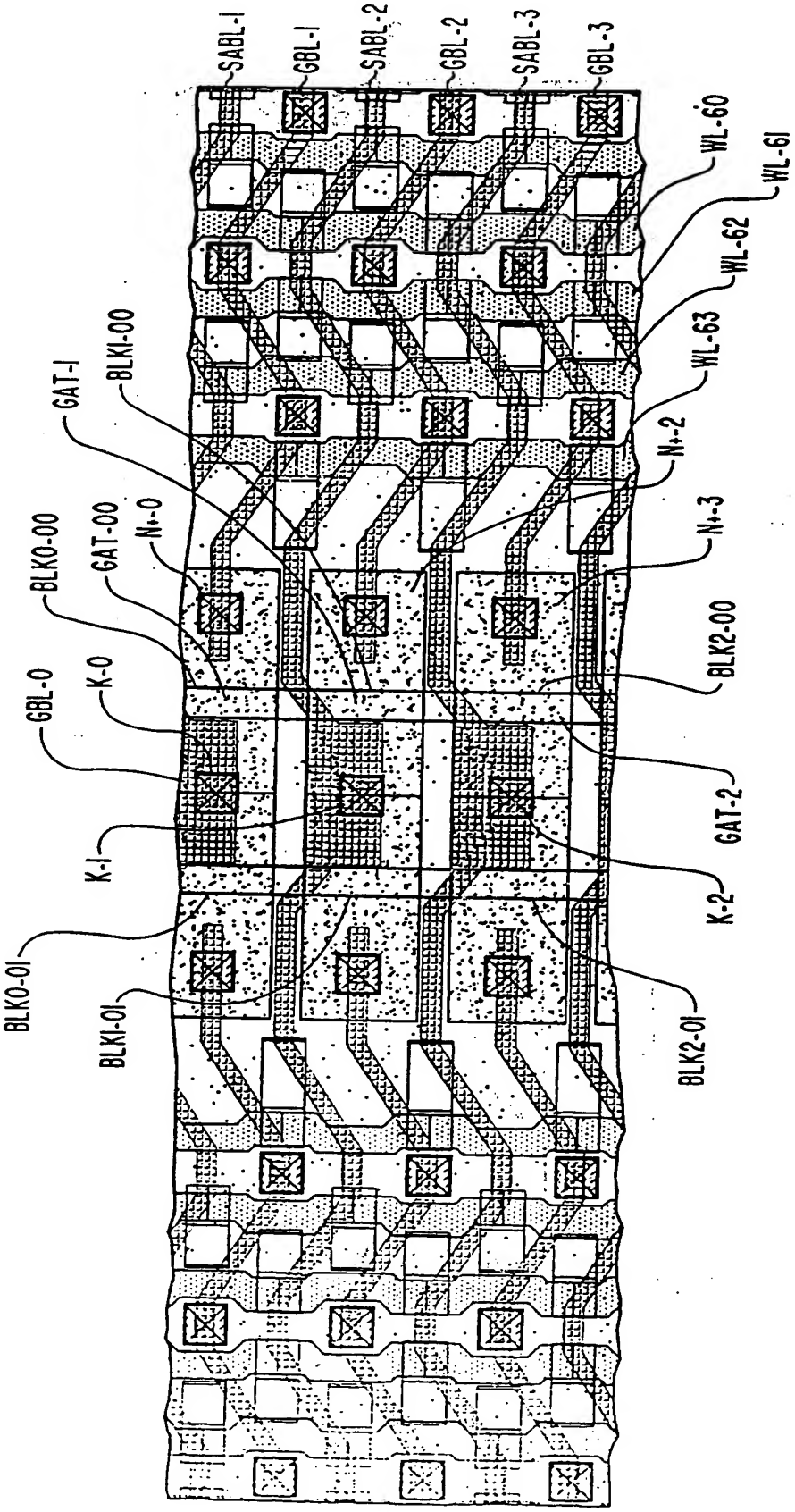
FIG. 6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GBL-1
SABL-2
GBL-2
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WL-60
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WL-63
N+-2
N+-3
BLK1-00
GAT-1
BLK0-00
GAT-00
N+-0
GBL-0
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K-1
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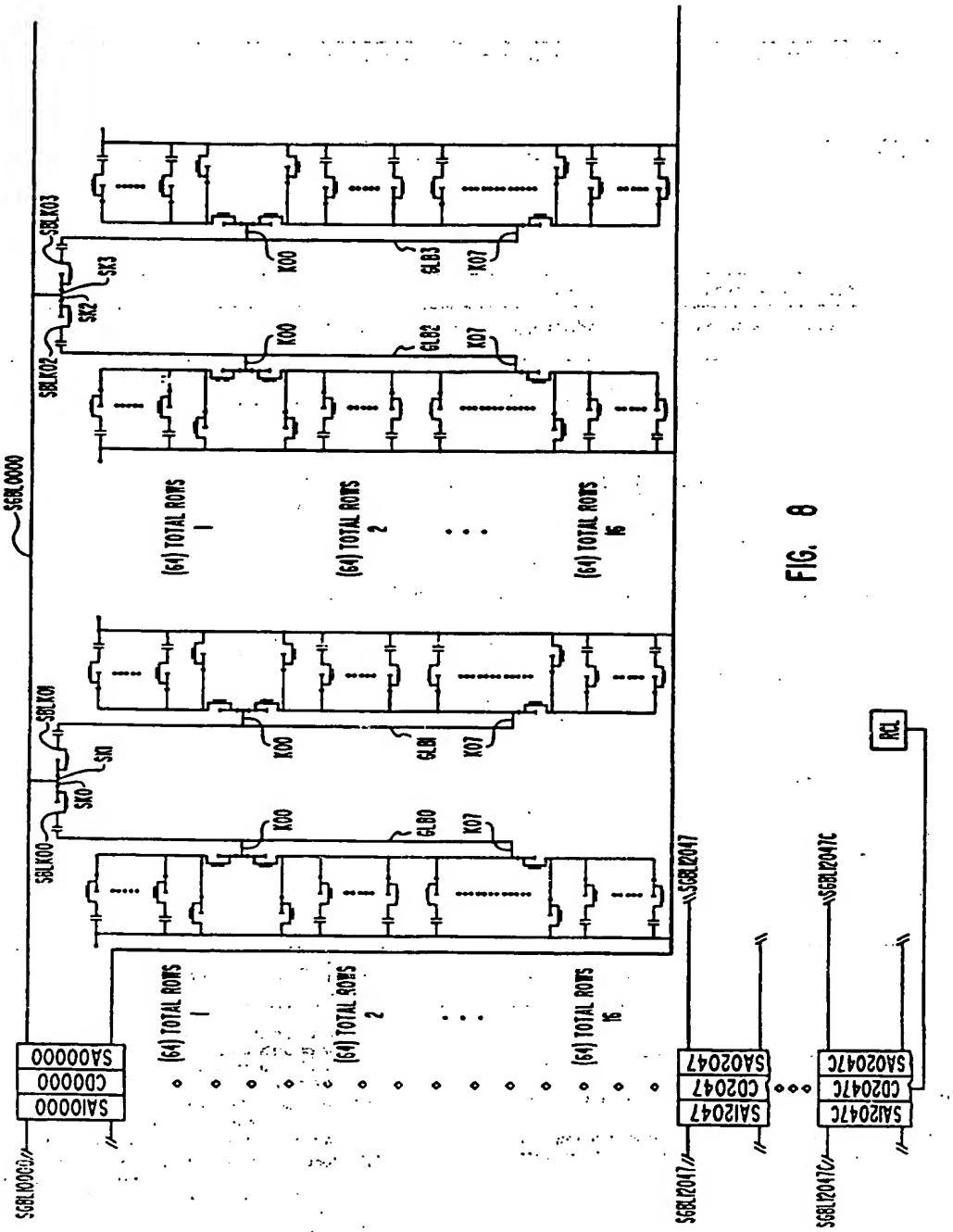
BLK1-01
BLK2-00
GAT-2
K-2
BLK2-01

FIG. 7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SBLK00
SX3
SX2
SX1
SX0
K00
K07
GLB3
GLB2
GLB1
GLB0
(64) TOTAL ROWS
1
2
16
SA00000
CD0000
SAI0000
SGBLK0000
SGBL2047
SA02047
CD2047
SAI2047
SGBL2047C
SA02047C
CD2047C
SAI2047C
RBL

FIG. 8

INTERNATIONAL SEARCH REPORT

Inte mal Application No
PCT/US 95/16071

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 593 152 (SUN MICROSYSTEMS) 20 April 1994 see column 4, line 33 - column 6, line 54	1,3,4, 6-8,11, 12
A	see column 9, line 31 - column 9, line 57; figures 2-5	5
X	US,A,5 361 233 (KOTANI) 1 November 1994 see column 6, line 38 - column 7, line 60; figures 3,4	1-3,6-8, 11,12
X	US,A,4 819 207 (SAKUI ET AL) 4 April 1989 see the whole document	1,3,6-8, 11,12

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 May 1996	22-05-96
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	**Authorized officer** Degraeve, L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 95/16071

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 056 811 (BAKER) 1 November 1977 see column 3, line 36 - column 4, line 45; figure 1	1,3,6-8, 11,12
A	EP,A,0 258 715 (NEC CORPORATION) 9 March 1988 see the whole document	1
A	US,A,4 636 988 (TRAN) 13 January 1987 see column 5, line 16 - column 5, line 59; figures 6,7	1,9
A	EP,A,0 101 884 (HITACHI) 7 March 1984 see the whole document	1
A	US,A,4 807 191 (FLANNAGAN) 21 February 1989 see the whole document	9,13,14

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PC I/US 95/16071

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		US-A-	5402386	28-03-95
		US-A-	5381377	10-01-95
US-A-5361233	01-11-94	JP-A-	4030385	03-02-92
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		JP-B-	3021996	25-03-91
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US-A-4807191	21-02-89	NONE		